

The diagram illustrates a display device architecture. At the top, a horizontal line is labeled "FIXED POTENTIAL LINE". Below it, a "TEST CIRCUIT" block (701) is connected to a series of scanning lines labeled S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11, S12, and Sn-1, Sn. The scanning line driving circuit (104) is shown on the left, with a vertical label "SCANNING LINE DRIVING CIRCUIT". It includes a series of transistors (6a, 7a, 8a, 9a) and capacitors (300, 3a) connected to the scanning lines. The data line driving circuit (101) is at the bottom, with a vertical label "DATA LINE DRIVING CIRCUIT". It includes a series of transistors (114, 116) and capacitors (118) connected to the data lines. The display area (115) is a grid of pixels, each containing a transistor (202) and a capacitor (301). Signal waveforms are shown for scanning lines G1, G2, and Gm, and data lines 114 and 116. A "FIXED POTENTIAL LINE" is also indicated at the top of the display area.

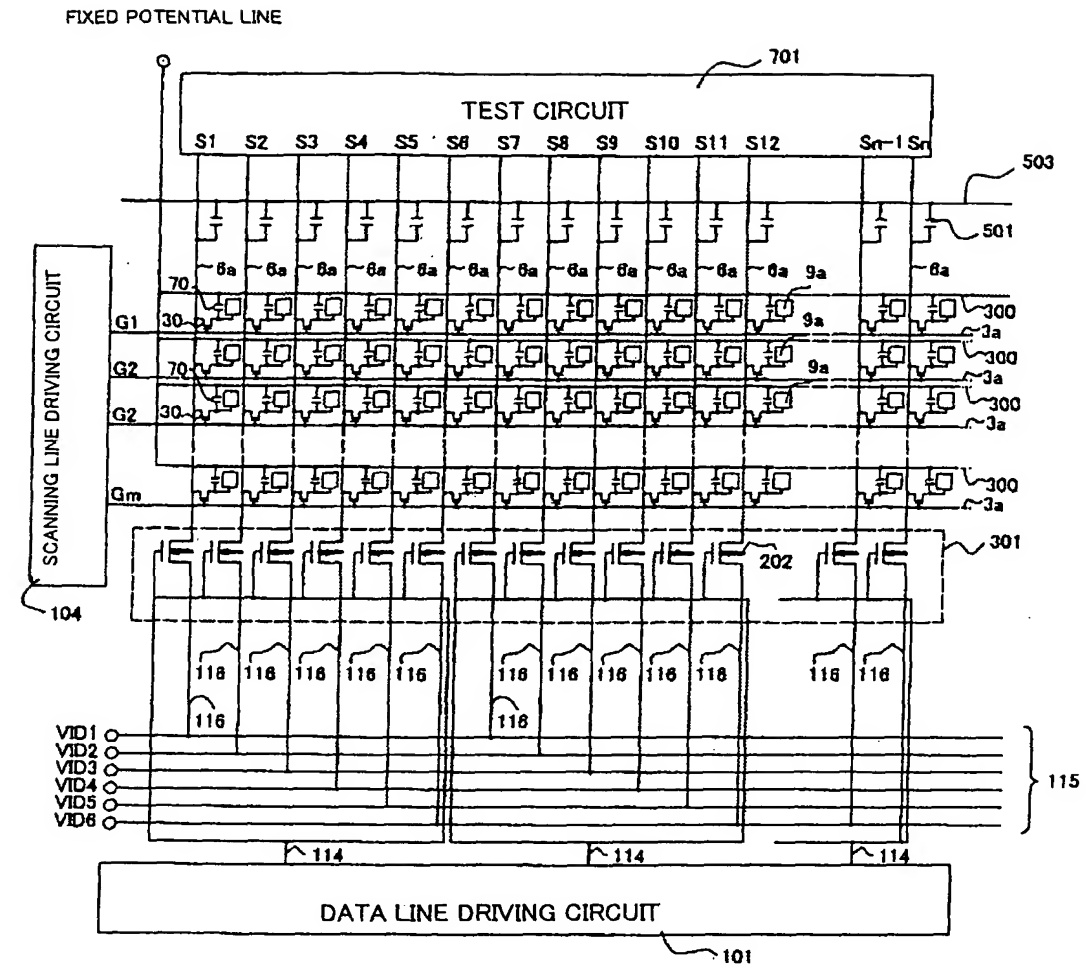


FIG. 2

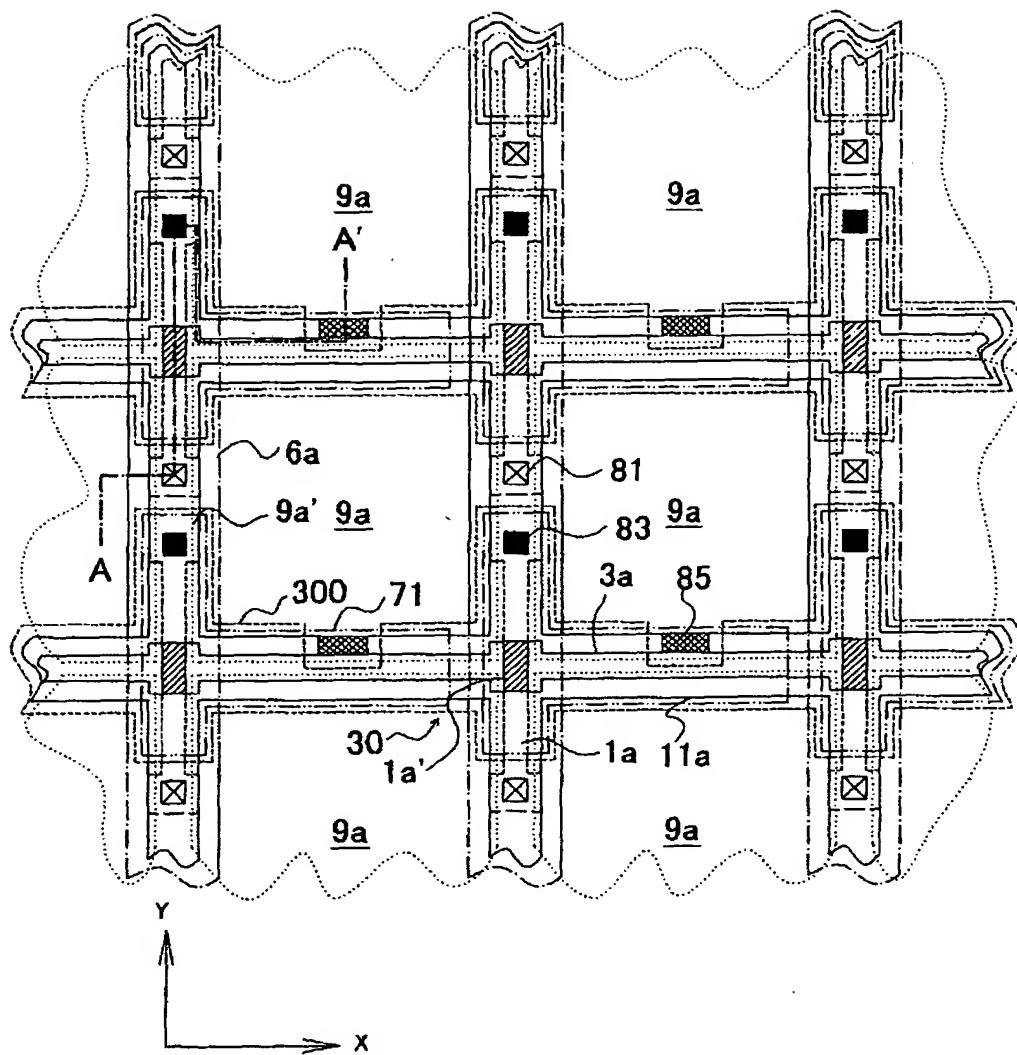


FIG. 3

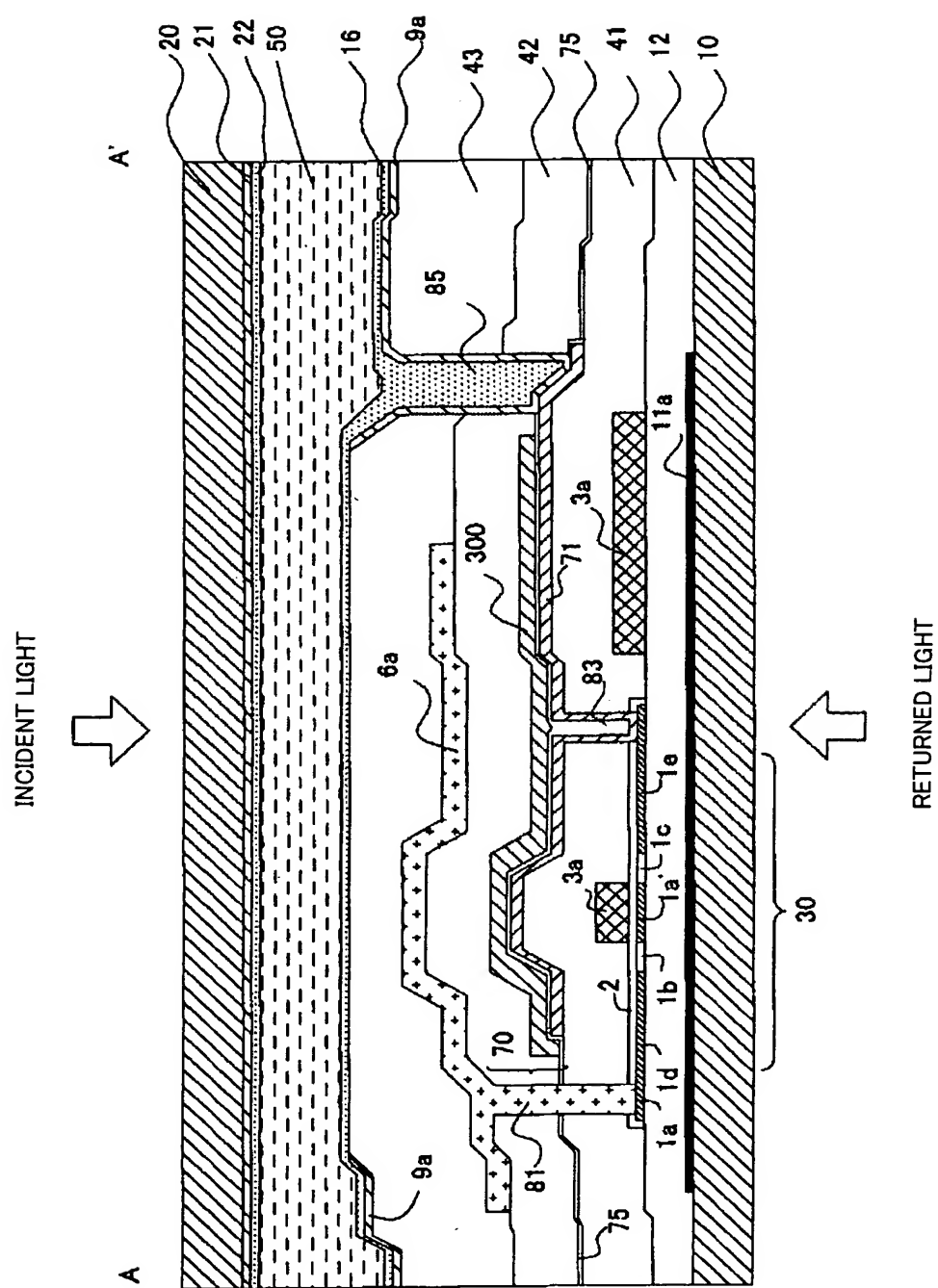


FIG. 4

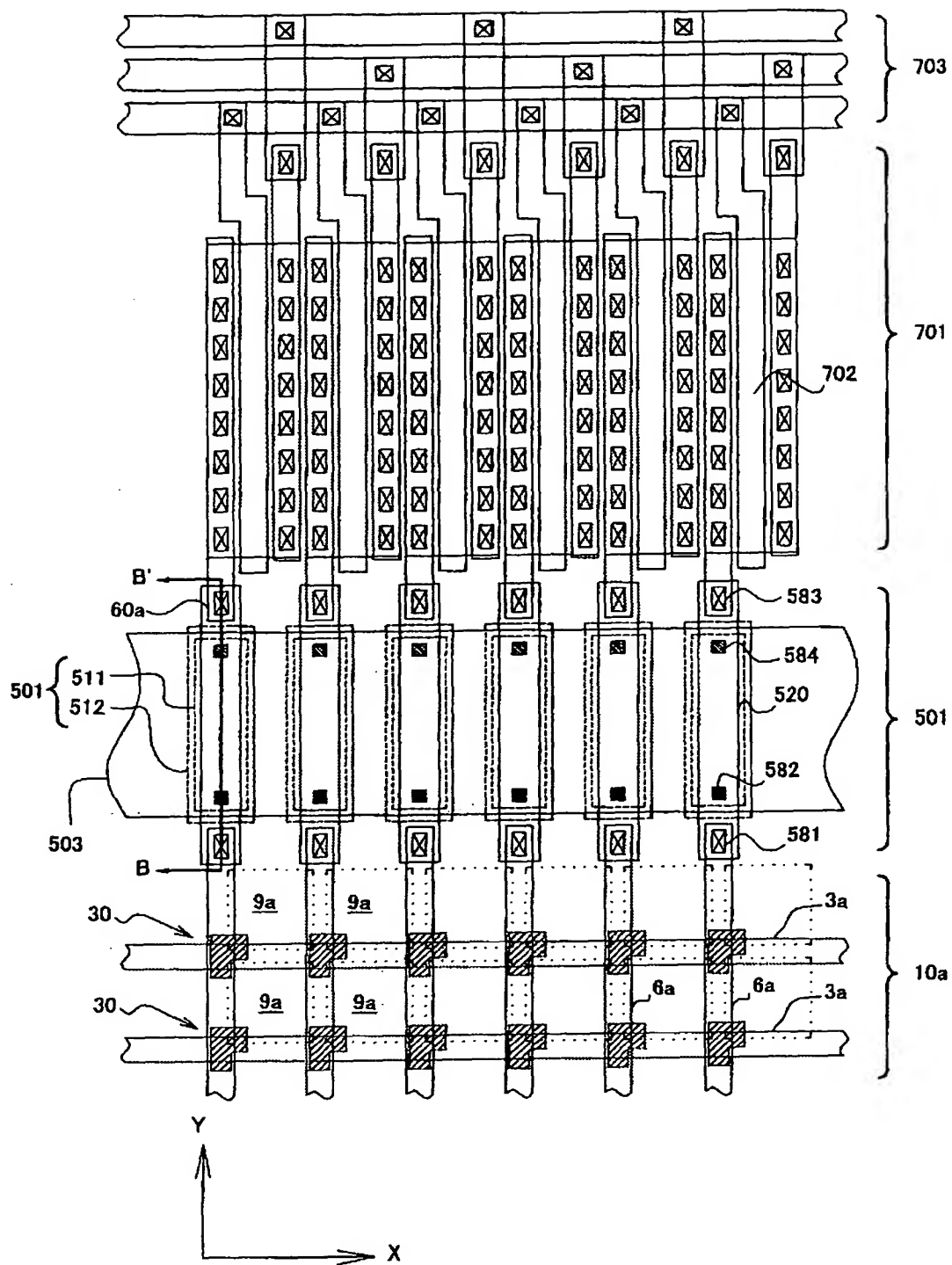


FIG. 5

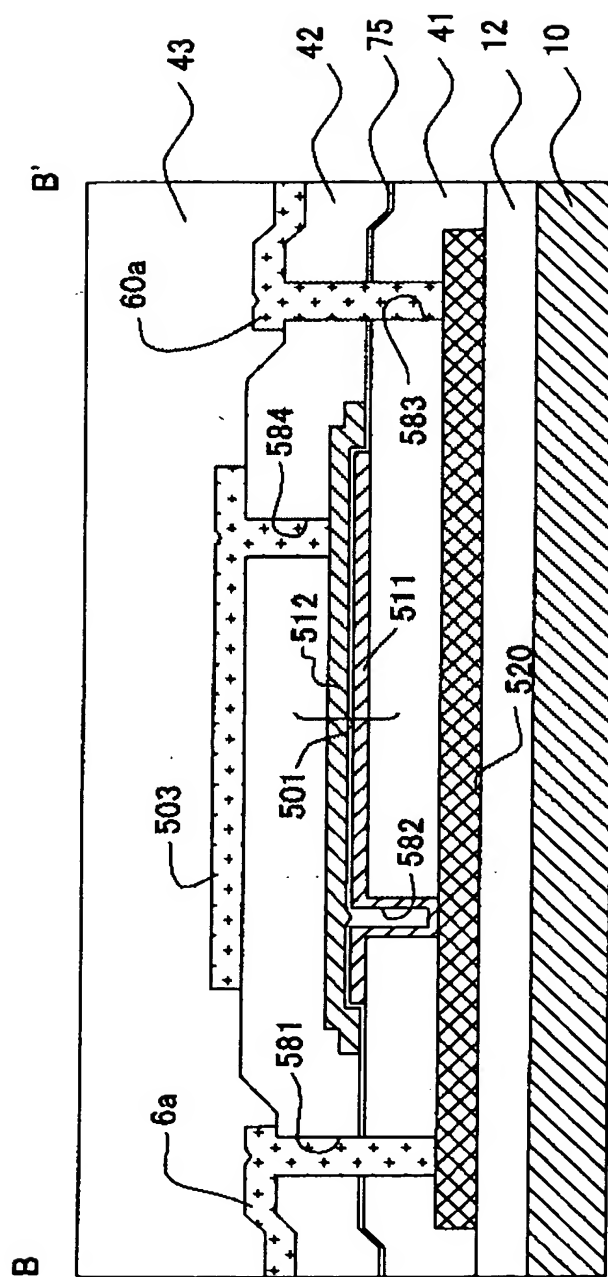


FIG. 6

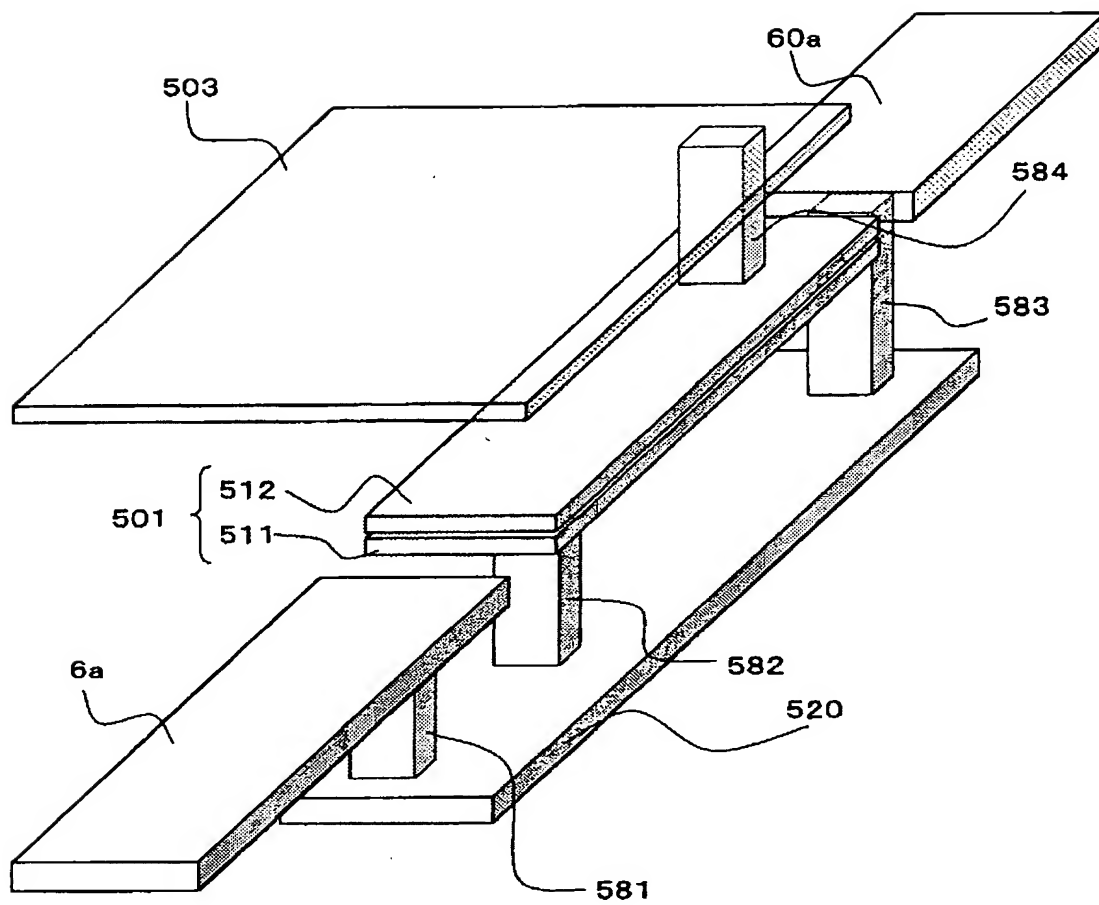


FIG. 7

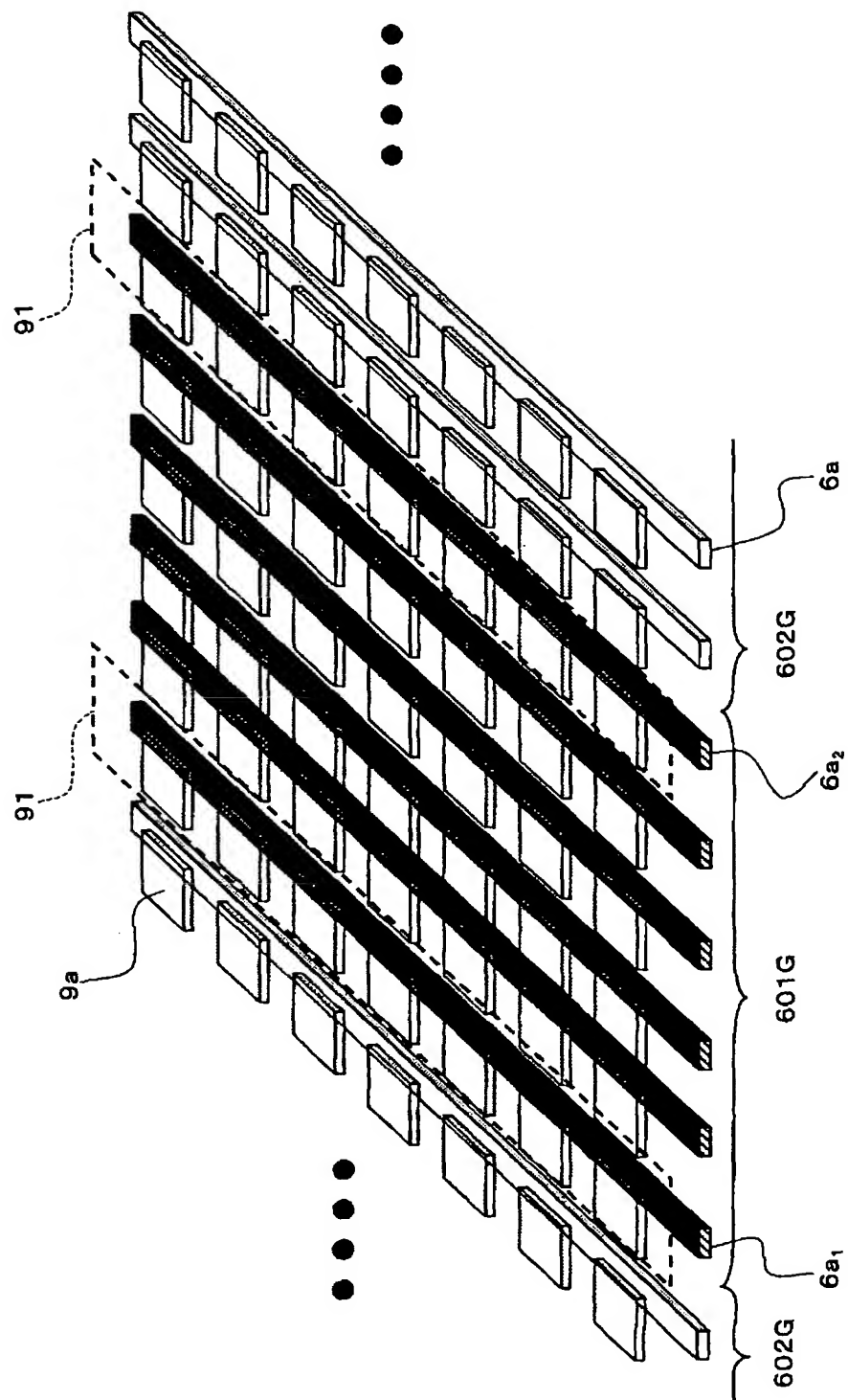


FIG. 8

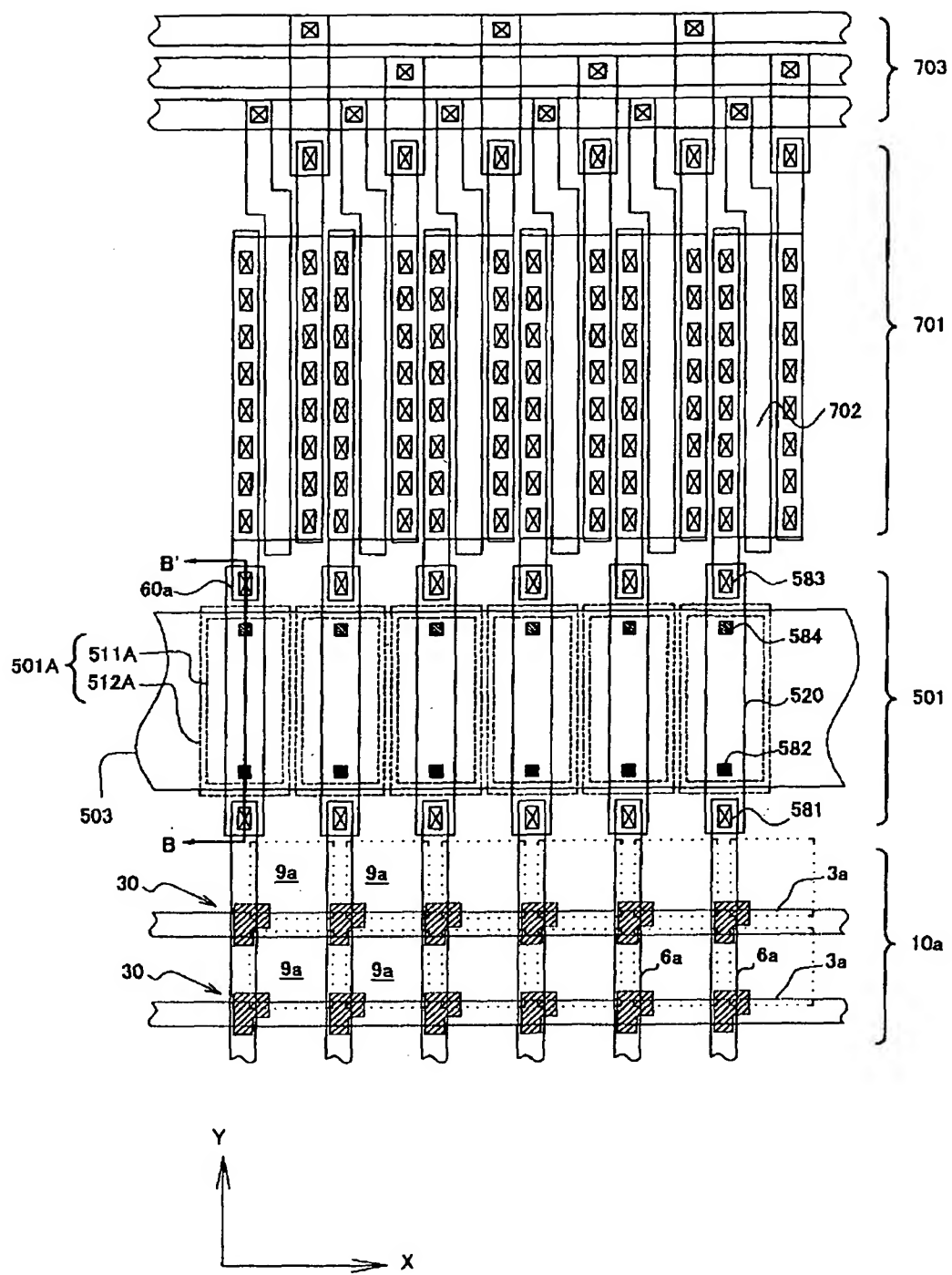




FIG. 9

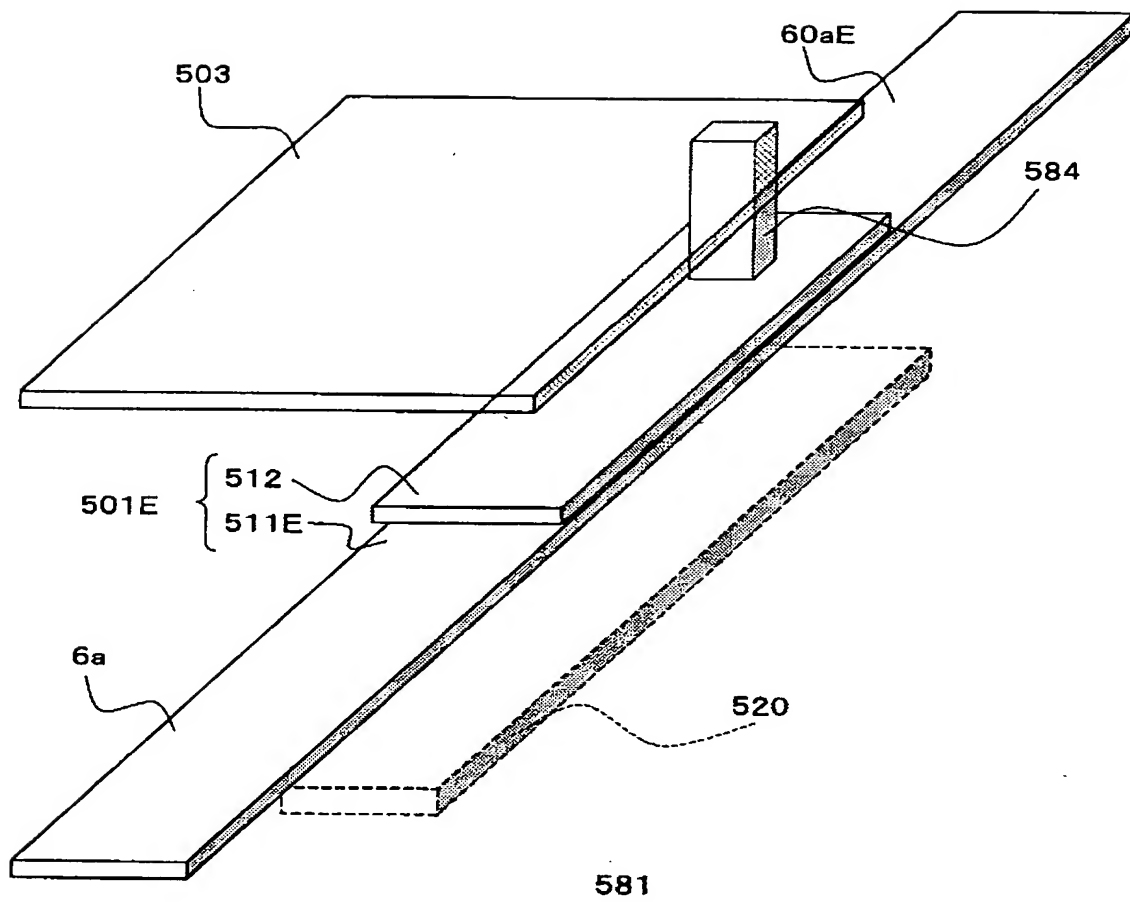
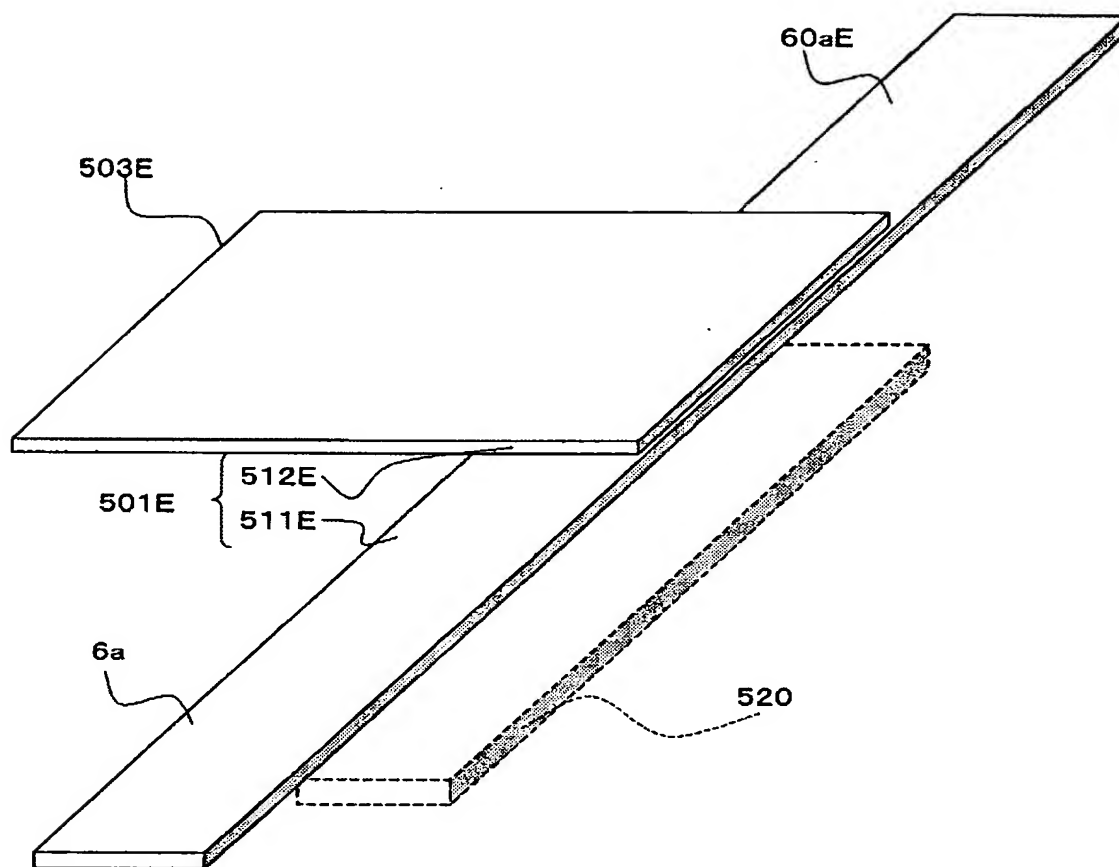
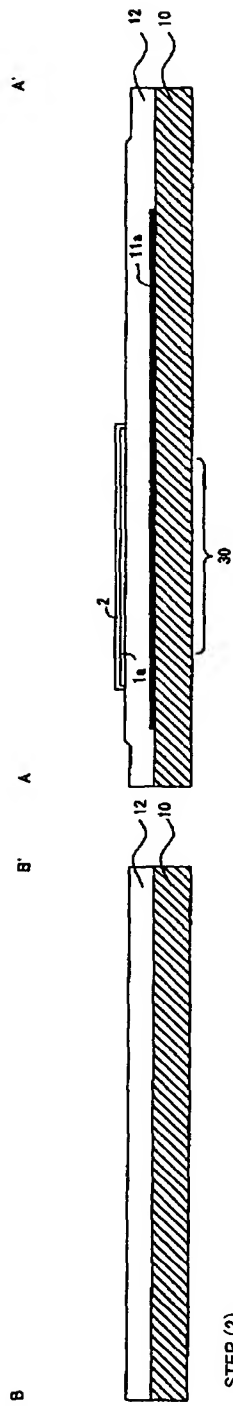


FIG. 10

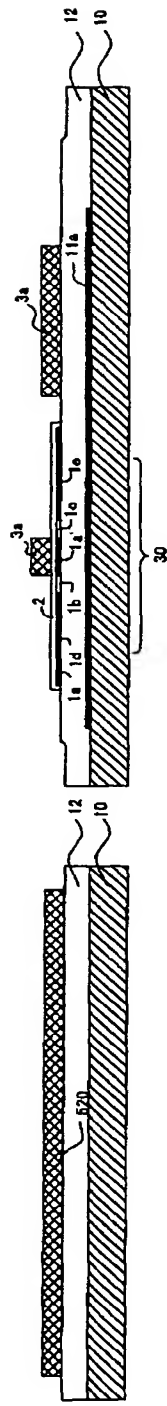


# FIG. 11

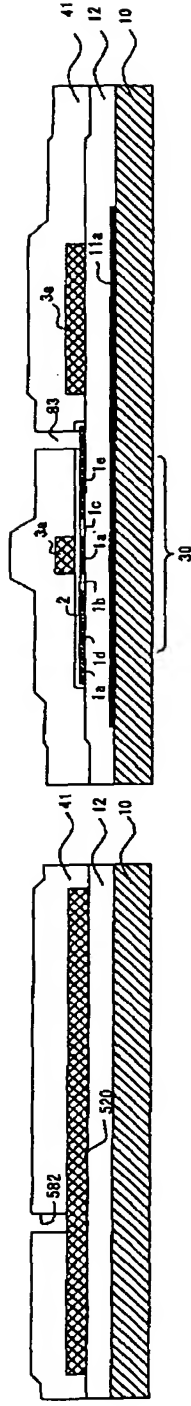
STEP (1)



STEP (2)



STEP (3)



STEP (4)

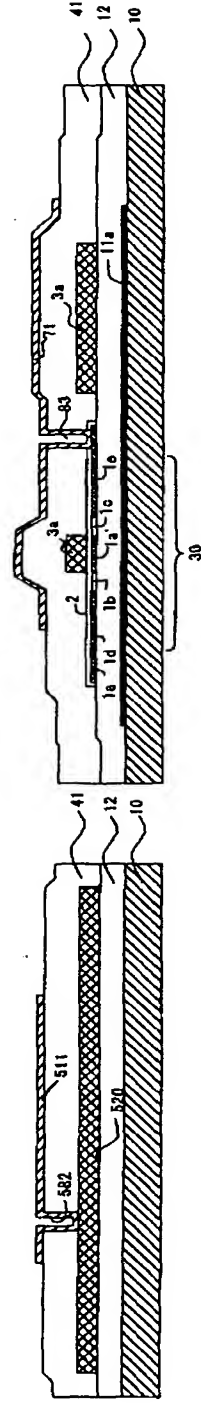


FIG. 12

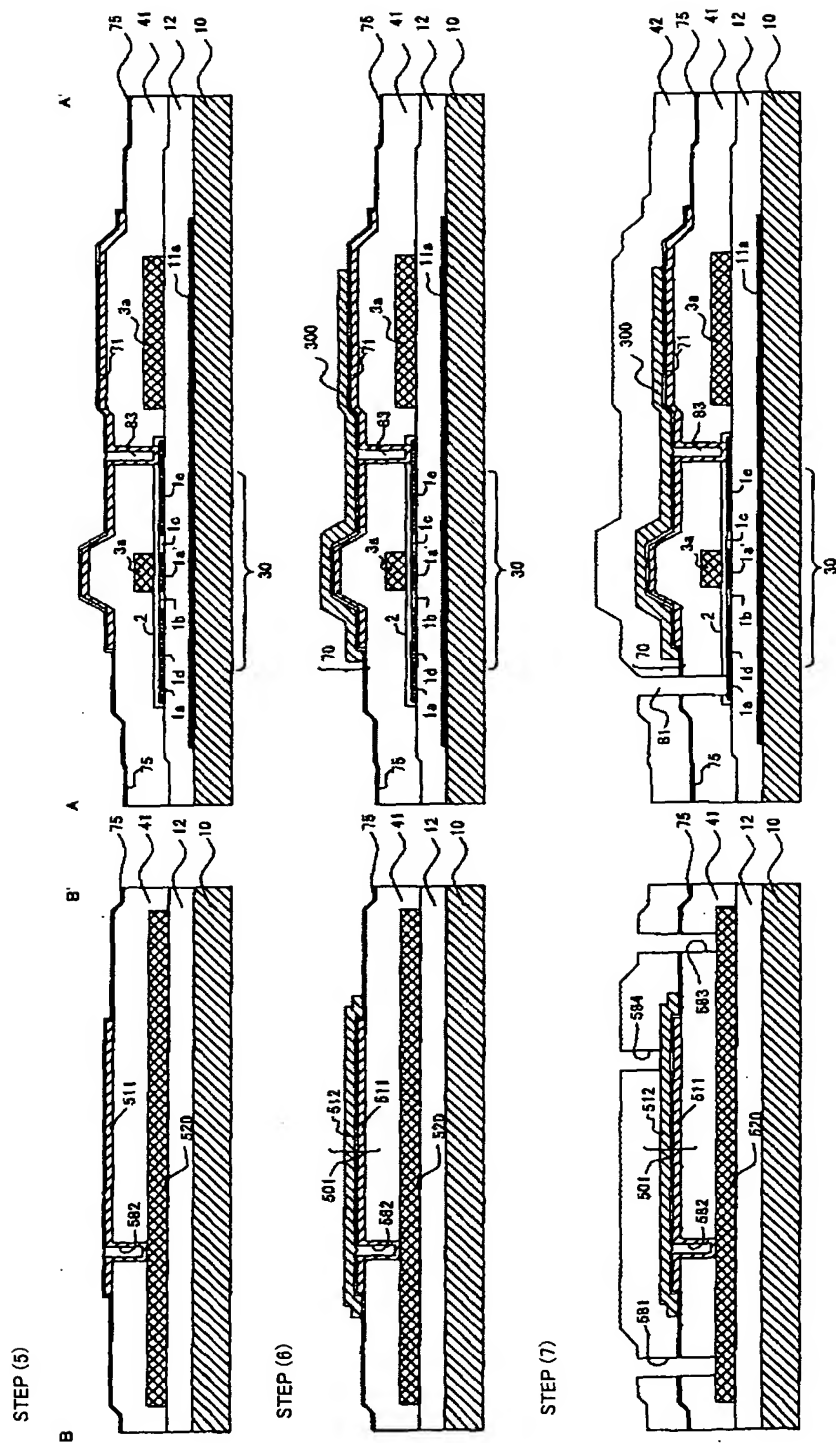


FIG. 13

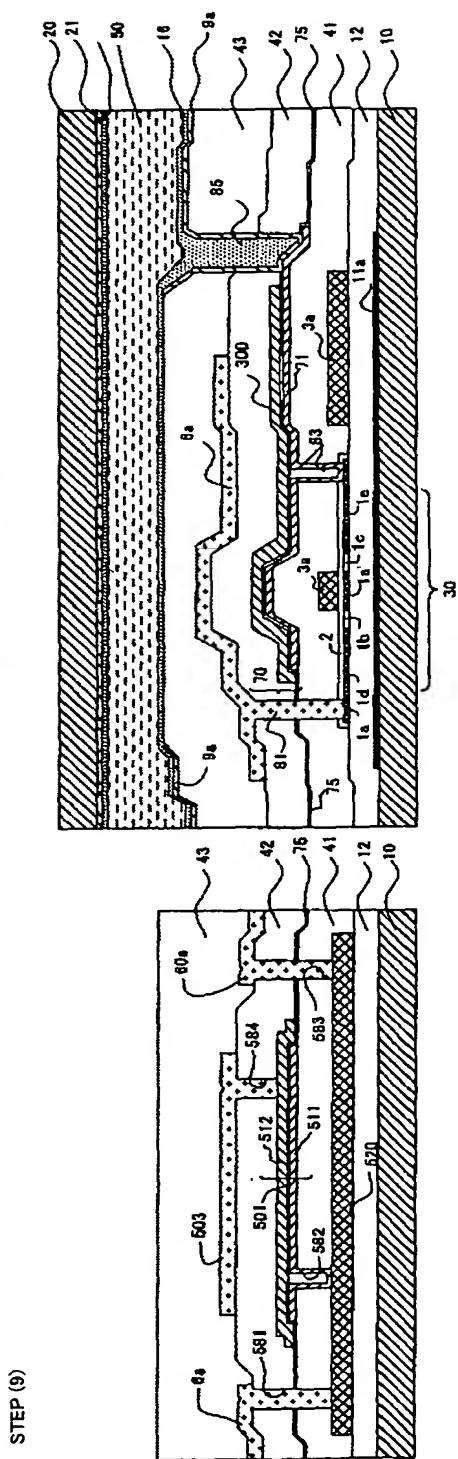
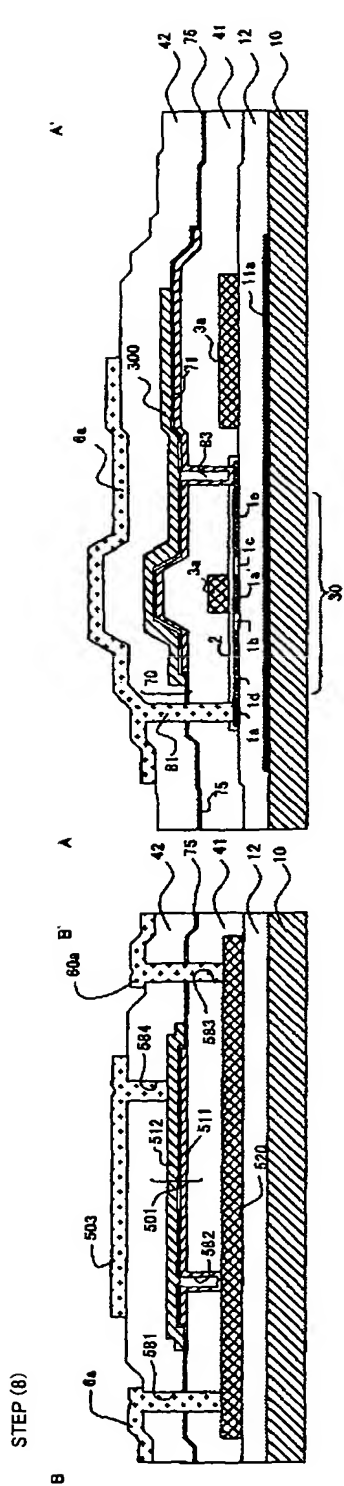


FIG. 14

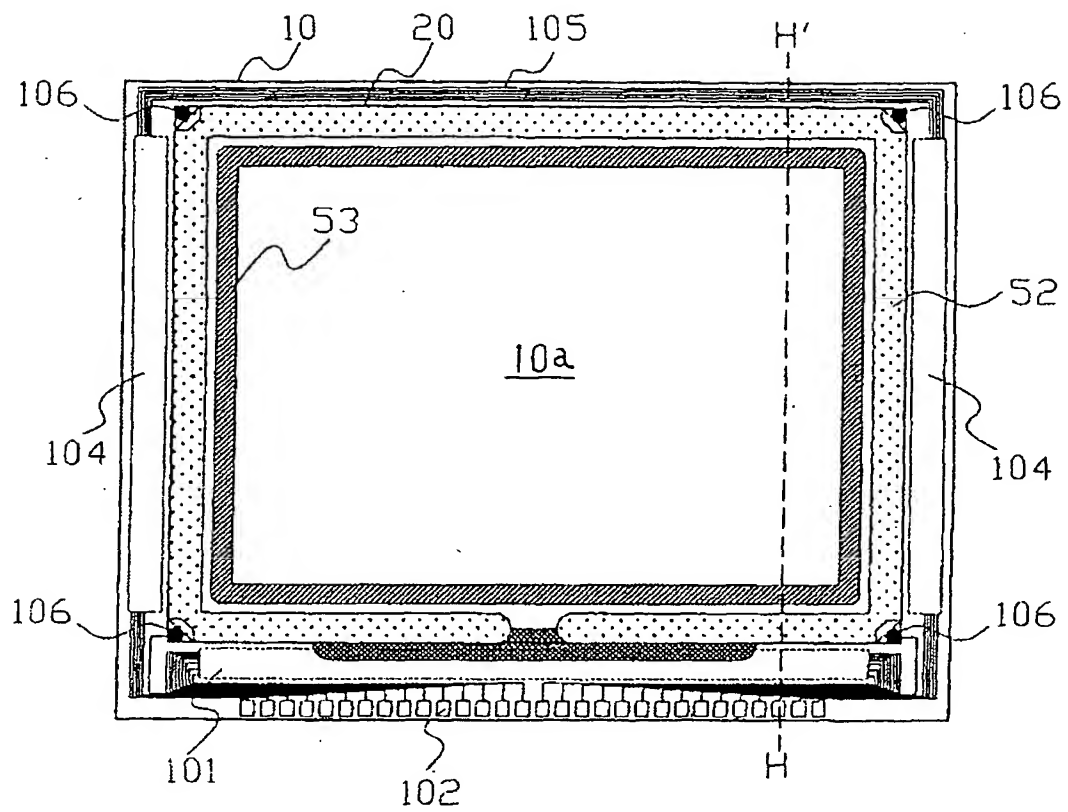


FIG. 15

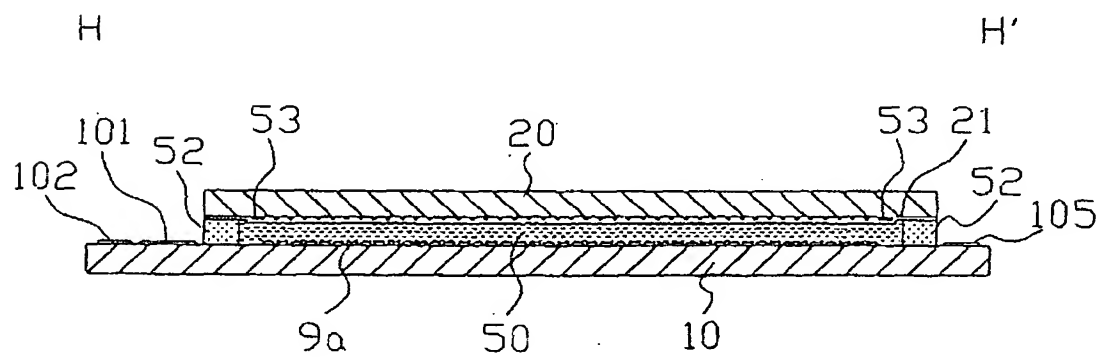


FIG. 16

